Dark Current Reduction in FF-CCDs

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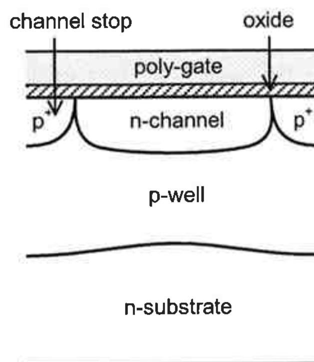
Abstract

Further dark current reduction in FF-CCDs used in professional digital still cameras is essential to obtain excellent pictures also at very long exposure times (~30s). This paper presents the implementation and results of a new 'all-gates-pinning' concept for integration in multi-pinned-phase mode. The dark current is reduced from 100 pA/cm^2 to 3 pA/cm^2 (16 e$^-$/pixel·s) at 60 °C and the associated fixed pattern noise is reduced with a factor of 8.

Introduction

The largest contribution of dark current and associated fixed pattern noise in our FF-CCDs is caused by interface states. The best method to reduce this contribution is by creating a hole layer at the entire interface, i.e. pinning the interface [1,2].
The introduction of a pinned layer at the interface during integration should not affect other CCD parameters such as quantum efficiency, maximum charge capacity, linearity, charge transport efficiency and angular response. In addition, two important features of our pixel design, vertical anti-blooming and electronic shuttering, should be maintained. The combination of large maximum charge capacity, vertical anti-blooming and electronic shuttering (with a maximum 10V pulse on the substrate) required a different approach than our former 'all-gates-pinning' (AGP) concept [3,4].



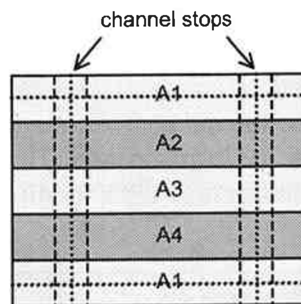


Fig. 1 a) Cross section perpendicular to transport direction of conventional image pixel. This buried channel CCD is formed by an n-channel implant on a profiled p-well on an n-substrate. p$^+$ channel stop implant separates the columns **b)** Top view of four-phase image pixel The four-phase approach allows highest charge capacity per area.

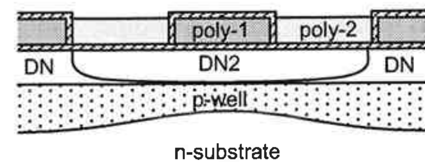


Fig. 2 Cross section along transport direction of non self-aligned AGP pixel (new concept). DN is the first n-channel implant and DN2 is the second channel implant (non self-aligned). The DN2 and p-well implant have been changed with respect to self-aligned AGP pixel.

AGP pixel design

3D off-state simulations were performed to find the optimal pixel design. Figure 1 shows a typical pixel without AGP: an n-channel implant in a profiled p-well on an n-substrate. The p+ channel stop implant separates the columns. The four-phase approach (fig. 1b) gives the highest charge capacity per area. Integration is done by collecting charge under three gates (high voltage level) and using one gate for separating the charge packets (low voltage level).
In the new AGP pixel design, the hole layer at the complete interface is obtained by putting all gates at a sufficiently low voltage level during integration. Consequently, the separation between charge packets needs

	Extra implant			
	n-type	p-type	self-aligned	non self-aligned
A	x		x	
B	x			x
C		x	x	
D		x		x

Table 1 The four different AGP concepts that have been simulated. The self-aligned implant is below two of four gates. The non self-aligned implant is below three integrating gates for n-type implant and below blocking gate for p-type implant.

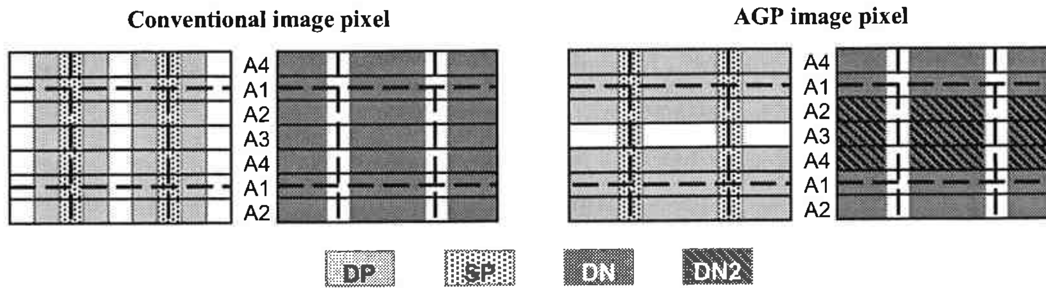


Fig. 3 Top view of channel stop implant (SP), p-well implant (DP) and n-channel implant (DN) for a conventional image pixel. Top view of rotated p-well implant and second n-channel implant (DN2) in combination with standard channel stop implant and n-channel implant for non self-aligned AGP image pixel.

to be built in by an additional p- or n-type implant. Four different concepts have been considered, see table 1. Option B, the extra n-type implant not self-aligned below three of four gates, gave the best simulation results and was selected for implementation in a test device. To maintain electronic shuttering functionality with a 10V pulse, it was necessary to rotate the p-well stripes by 90° compared to the standard pixel layout. This new AGP pixel design is plotted in figures 2 and 3. In figure 4a, the simulation result of a neighboring filled and empty AGP pixel is plotted when all gates are at the same low voltage level. The charge packet of the filled pixel is clearly separated from the empty pixel, the holes at the surface and the substrate. In figure 4b the potential profiles for empty pixel, blocking gate and electronic shutter conditions are shown.
According to simulations a misalignment of 0.25μm for the non self-aligned implant (i.e. larger than the maximum process tolerance) does not compromise the performance. The misalignment opposite to the vertical transport direction is most critical for good transport, while a misalignment in the transport direction

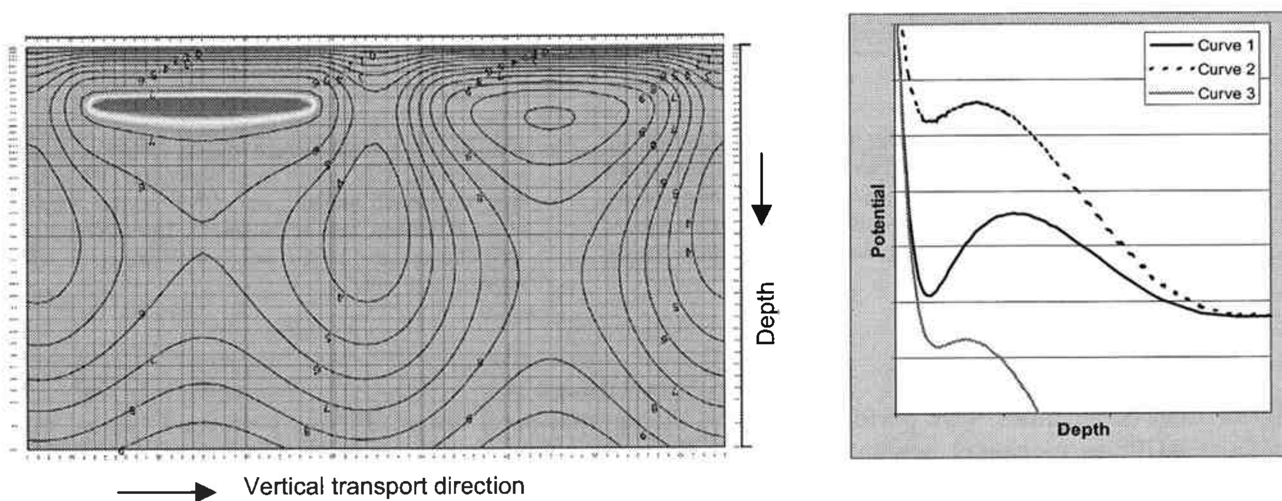


Fig. 4 Simulation results of the new AGP pixel design. **a)** Cross section of two pixels (one full and one empty) in the center of the channel along transport direction showing the potential contour lines and the electrons in the filled pixel. **b)** Potential profiles: *Curve 1*: below integrating gate (A3) with empty well. *Curve 2*: below blocking gate (A1). *Curve 3:* under electronic shutter conditions.

Parameter	Original Sensor	Sensor with AGP
n-substrate voltage	25 V	24 V
electronic shutter pulse	10 V	10 V
maximum charge capacity	100 ke$^-$	50 ke$^-$
dark current @ 25 °C	7 pA/cm^2	0.3 pA/cm^2
FPN @ 25 °C	11 pA/cm^2	4.5 pA/cm^2
dark current @ 60 °C	100 pA/cm^2	3 pA/cm^2
FPN @ 60 °C	140 pA/cm^2	16 pA/cm^2
sensitivity red @ 650 nm	1.0 R a.u.	1.1 R a.u.
sensitivity green @ 550 nm	1.0 G a.u.	1.0 G a.u.
sensitivity blue @ 450 nm	1.0 B a.u.	1.0 B a.u.

Table 2 CCD parameters obtained with an original 4M pixel sensor and with a 4M sensor with the AGP non self-aligned pixel design.

improves the transport. Since transport should be possible in both directions, an offset of the extra DN implant was not allowed.

This extra n-implant is only a minor change in our CCD process. Only one extra mask is necessary, the required implant energy and thermal budget are equal to the first n-implant.

Results

In table 2 the results obtained with this AGP design in a 4M sensor with 9µm pixels are summarized. The dark current and FPN (which were already competitively low) are reduced enormously, electronic shuttering

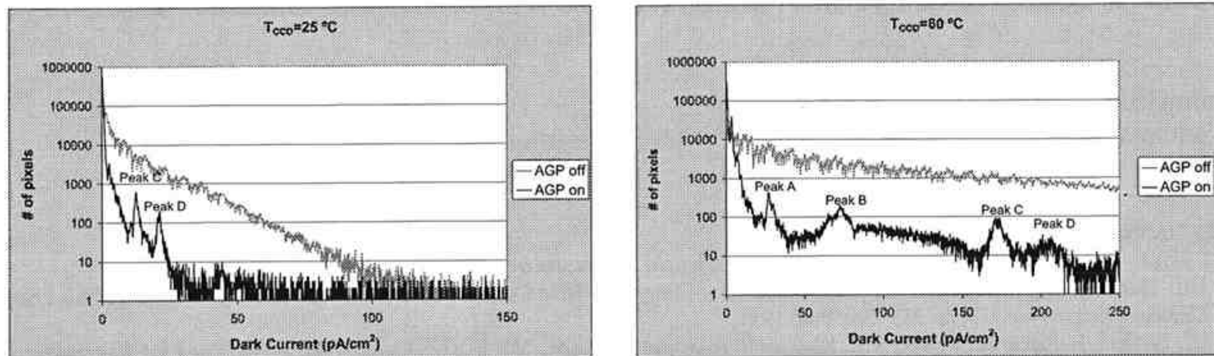


Fig. 5. Histogram of dark current at 25 °C and at 60 °C of a 4M sensor with the AGP non self-aligned pixel design with AGP off and on. Integration time was 30s.

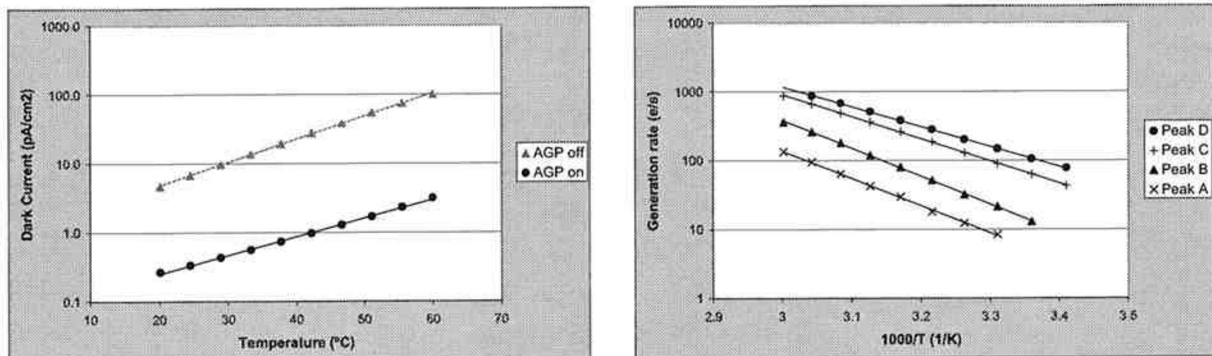


Fig. 6 Average dark current as function of CCD temperature for a 4M sensor with the AGP pixel design with AGP on and off. For 'AGP on' the dark current doubles per 11 °C and for 'AGP off' per 9 °C.

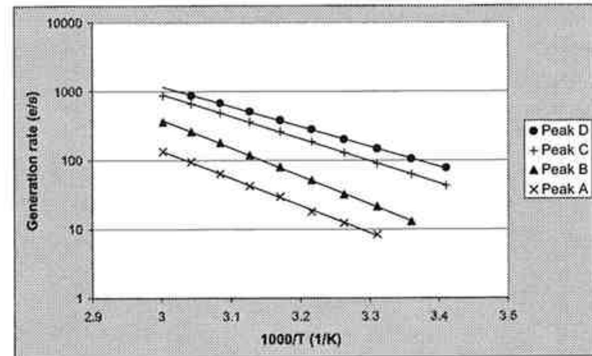


Fig. 7 Temperature dependence of deep level traps observed in the dark current histogram.

is as before obtained with a 10V pulse, sensitivity is unchanged and transport efficiency is not affected even with a 0.25µm misalignment of the extra n-implant. The maximum charge capacity is reduced by 50%.

Figure 5 shows the histogram of the dark current at 25°C and 60°C for the sensor with AGP mode 'on' and 'off'. The tail of the dark current is enormously reduced and peaks of deep level traps are now well detectable. In figure 6 the temperature dependence of the average dark current is plotted. Without AGP the dark current doubles per 9°C and with APG mode 'on' the dark current doubles per 11°C. In figure 7, the temperature dependence of the deep level traps is shown and in table 3 the generation rate and activation energies for these traps are summarized. Based on the analysis of metal traps in CCD image sensors by McColgin et al [5], Au and Pt are the suspected metal contaminants for traps C and D respectively.

Trap	**Generation Rate** (e^-/s at 60 °C)	**Activation Energy** (eV)
Peak A	134	0.79
Peak B	363	0.81
Peak C	873	0.64
Peak D	1017	0.58

Table 3 Properties of deep level traps observed in dark current histogram.

Conclusions

Concluding, this new concept of 'all-gates–pinning' offers a dark current reduction of a factor 30 without affecting other CCD parameters. The required extra n-implant is a minor change in our CCD process and the non self-aligned design was proven to be robust. The maximum charge capacity was reduced by a factor 2, but a larger capacity is feasible by optimizing the implants.

The achieved dark current of 3pA/cm^2 (16e/pixel·s) at 60°C is the best reported in literature so far.

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